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X, Ku-BAND GaAs MONOLITHIC AMPLIFIER*

Y. Tajima, T. Tsukii†, E. Tong, R. Mozzi, L. Hanes, B. Wrona
Research Division, Raytheon Company
131 Spring Street
Lexington, Massachusetts 02173

†Electromagnetic Systems Division
Goleta, California 93017

Abstract

A two-stage X-, Ku-band monolithic FET amplifier has been developed. Initial results indicate a gain of 7-10 dB across the 8-20 GHz band with a typical rf power output of 100 mW. A balanced amplifier consisting of two two-stage amplifiers and a pair of Lange couplers yielded 10.5 ± 1 dB gain from 7.5 to 18 GHz and an output power of 150-250 mW in Ku-band.

Introduction

Broadband GaAs monolithic amplifiers operating in X-band or below have been reported[1-5] and a few papers discuss monolithic amplifiers which operate over a narrow range in Ku-band. In this paper, we will describe the design, fabrication, and performance of broadband amplifiers which operate in both X- and Ku-band. These results are the first demonstration of broadband monolithic amplifiers in this frequency range.

Amplifier Design

The circuit topology of the two-stage amplifier is shown in Fig. 1. The amplifier consists of input matching section, first FET, interstage matching circuit, followed by second FET and output matching section.

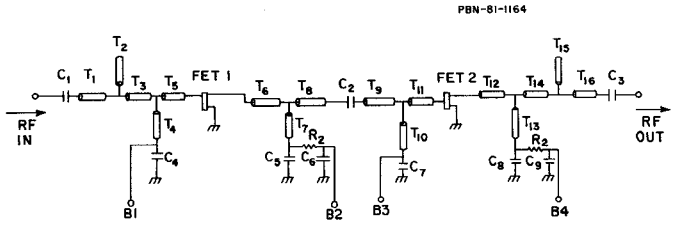

Fig. 1 Circuit topology of the two-stage amplifier.

First and second FETs have been selected as 200 μm and 400 μm respectively to achieve 100 mW of rf level across 7-18 GHz frequency band.

Equivalent circuit model of both FETs were derived from the extrapolation of other submicron gate discrete devices previously developed.

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Restrictions imposed upon the monolithic integrated circuit for selecting values of each passive element were carefully considered and incorporated into the amplifier design. For example, each capacitor varies from sub-picofarad to several picofarad based upon dc blocking or rf bypass requirements and upon their compatability with other adjacent passive element interfaces. By the same token, individual microstrip transmission impedance varied from 44 to 80 ohms.

Computer aided design program, COMPACT, has been used in optimizing matching elements coupled with passive elements.

Thin-film Ti resistors were used to improve the gain flatness in the band; i.e., large amounts of available gain were absorbed in the resistors in the low-frequency region and these resistors had hardly any effect at high frequencies. Thin film Si_3N_4 capacitors were used for matching elements as well as dc blocking and bypass capacitors. Rf shorted stubs terminated by large bypass capacitors were used for dc bias lines.

Figure 2 is the photograph of a two-stage amplifier chip. It should be noted that the signal path has been laid out in a meander pattern to make a dense circuitry. Such a layout also offers flexibility in determining chip size with a goal of achieving low aspect ratio in mind. The chip size is 2.6 × 2.3 mm.

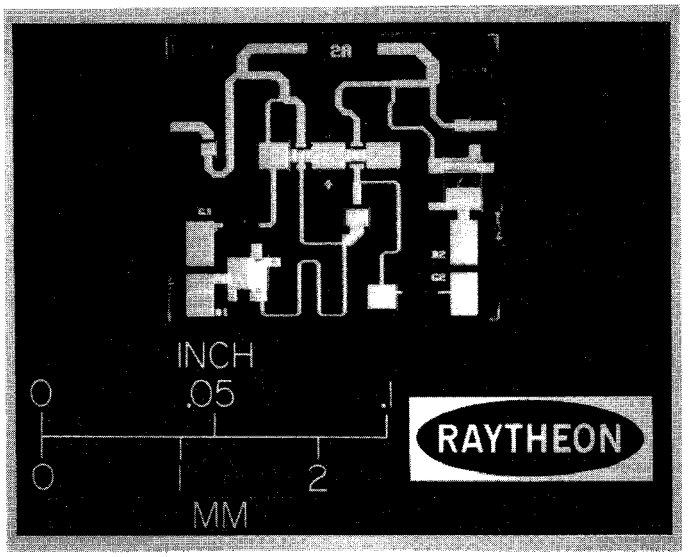

Fig. 2 Photograph of a two-stage amplifier chip.

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Circuit Fabrication

The circuits were made on vapor-phase-deposited n-type epilayers grown on semi-insulating substrates. The epilayers consisted of a 0.2 μm thick n^+ contact layer (10^{18} -10^{19} carriers/cm^3) over a 0.4 μm thick n active layer (1.7×10^{17} carriers/cm^3) on a 2 μm thick buffer layer. Source and drain contacts for the FETs, and the bottom metal of dielectric capacitors consisted of an alloyed NiAuGe composite. Transmission line capacitor tops were TiAu films gold-plated to a thickness of about three microns. Contact pads and air bridges were plated at the same time. After thinning the backside of the wafer, via-holes were etched to the FET source contacts and a ground plane evaporated and gold-plated. Completed wafers were diced into chips, and each chip with acceptable dc parameters was die-bonded on a carrier and placed on a test fixture to make rf measurements.

Two kinds of FETs with total gate periphery of 200 μm and 400 μm respectively were used in these amplifiers. All the gate fingers (TiPtAu) were 0.7-0.8 μm long and 100 μm wide and were recessed through the contact layer and partially into the active layer. An air bridge was used to connect source contacts on the 400 μm periphery FET. An SEM photograph of this type FET is shown in Fig. 3.

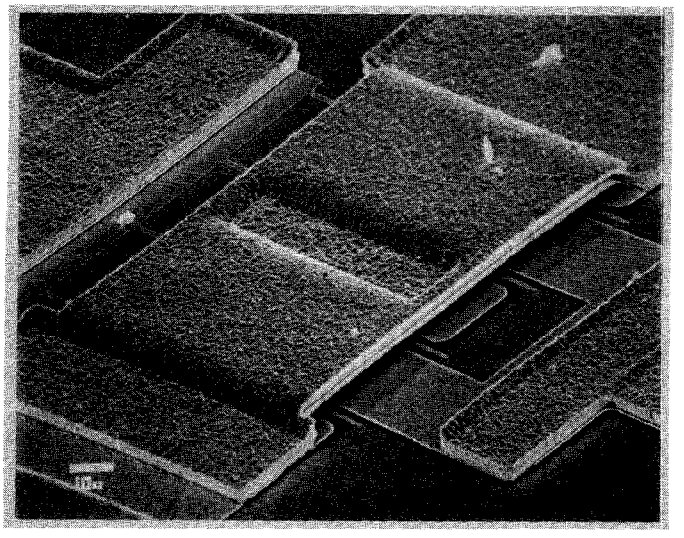

Fig. 3 SEM photograph of a 400 μm FET used in the amplifier.

Rf Performance

Figure 4 illustrates the small-signal gain performance of a two-stage amplifier, along with input/output return loss over the 6-21 GHz range. There is 7-10 dB gain across 8-20 GHz with a good match to the output and an input match monotonically improving with increasing frequency. The overall gain, however, is 1 dB lower than the predicted design data, and the amplifier gain has a tendency to dip around 10 GHz. Both discrepancies are due to the difference between GaAs FET models used for the design and actual device parameters which were later derived from the discrete FET S-parameters obtained by de-embedding techniques.

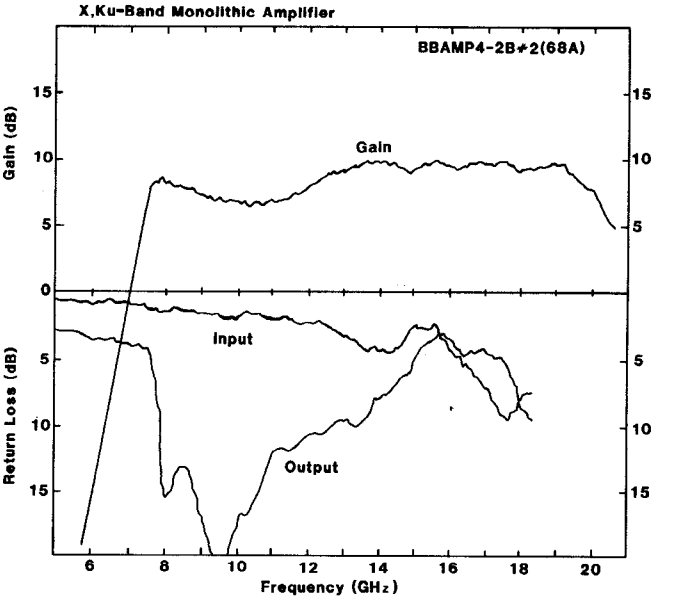

Fig. 4 Small signal performance of a two-stage monolithic amplifier.

A balanched amplifier was constructed by combining two monolithic chips and 3 dB hybrid couplers fabricated on 15 mil thick alumina substrates. A photograph of the balanced amplifier module is shown in Fig. 5.

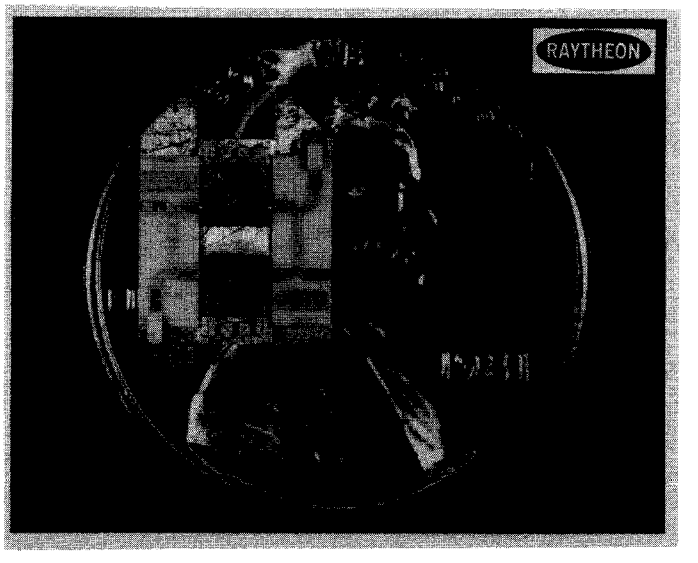

Fig. 5 Balanced amplifier module.

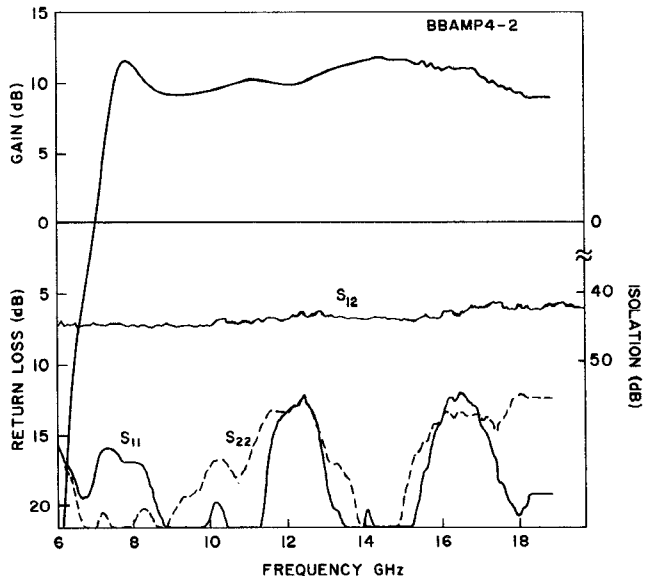

Fig. 6 Small signal performance of a balanced amplifier module.

The module showed excellent performance with 10.5 ± 1.0 dB gain across 7.5 to 18.6 GHz (Fig. 6). Note also the outstanding input/output VSWRs as well as the high reverse isolation. The module was exposed under swept power measurements which resulted in +21 to +23 dBm at 1 dB compression level for X-through Ku-band. Figure 7 shows the power transfer characteristics taken at 15 and 18 GHz. No tweaking was done on any of these chips and the chips were only selected based on dc data.

Conclusions

Monolithic, medium-power, two-stage amplifiers for X-, Ku-band frequency coverage have been successfully designed, fabricated and demonstrated. We have also proven that these monolithic chips can be integrated with hybrid couplers to form a balanced amplifier.

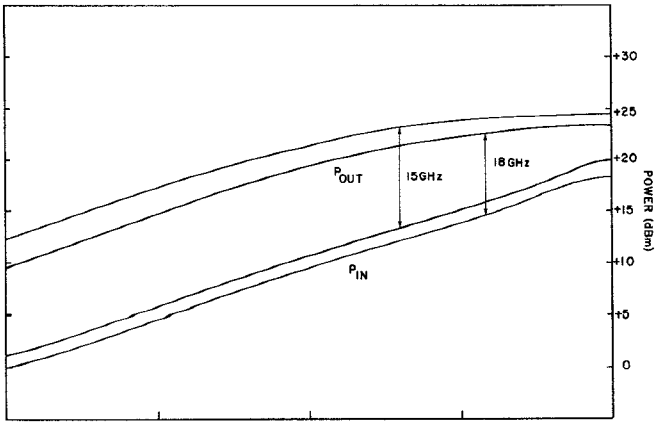

Fig. 7 Power performance of a balanced amplifier module.

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